Digital Circuits

ECS 371

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Lecture 15

Office Hours:
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Some questions...

- Is the exam too difficult?
- Is the exam too long?

Announcement

- Reading Assignment:
  - Chapter 7: 7-1, 7-2, 7-4

Digital Logic Circuit Types

- Combinational Circuit
  - Output depends only on current inputs
  - No feedback loops
  - "memoryless"
- Sequential Circuit
  - Output depends on past history plus current inputs
  - Contains feedback loops
  - Has memory

- Up to this point, we have focused on "**combinatorial logic circuits**" (i.e. the output of the circuit is dependent on the current input ONLY).
- Now we will shift our focus to "**sequential logic circuits**" (i.e. the output depends not only on the present input but also on the **history** of the input.
- The basic building blocks for sequential logic circuits are "**latches**" and "**flip-flops**"

Sequential Logic Circuits

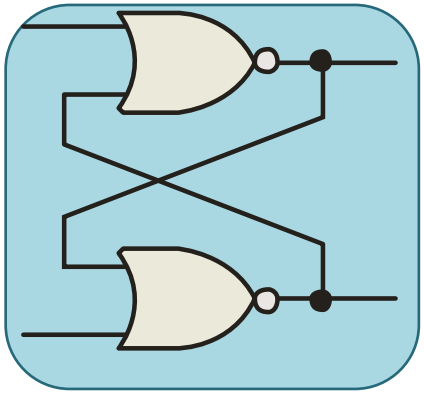
- Memory is represented in the form of states.
- "State" embodies all the information about the past needed to predict current output based on current input.
- State variables are one or more bits of information representing logic signals in a circuit
  - Tell you "where the circuit is"
  - Used in conjunction with inputs to derive current outputs of a sequential circuit
- In combinational circuits, only need to look at the current inputs to get the current output.

Exercise

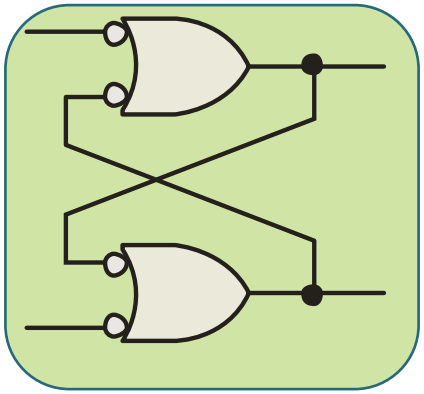
- Separate into a group of two persons.
- Can you come up with a simple device that is a good example for sequential circuit?

S-R Latch

- A **latch** is a temporary storage device that has two stable states (bistable). It is a basic form of memory.
- The **S-R (Set-Reset) latch** is the most basic type.
  - It can be constructed from NOR gates or NAND gates.
  - With two cross-coupled **NOR gates**, the latch responds to **active-HIGH inputs**.

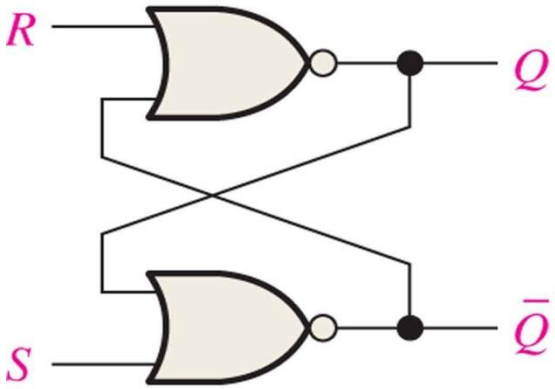


  - With two cross-coupled **NAND gates**, the latch responds to **active-LOW inputs**.

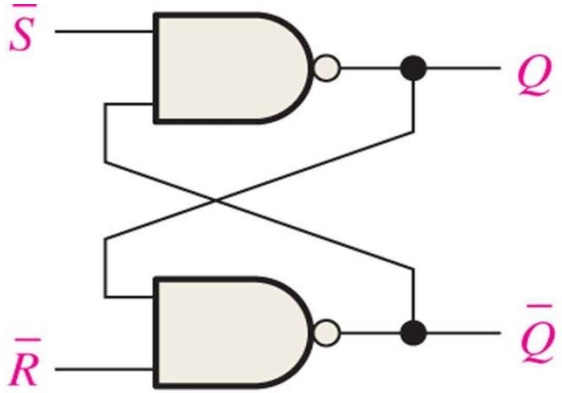


S-R Latch

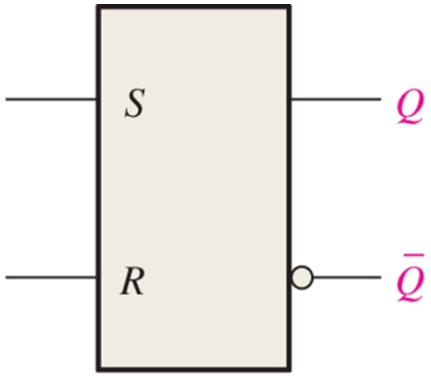
- There are two versions of SET-RESET (S-R) latches.

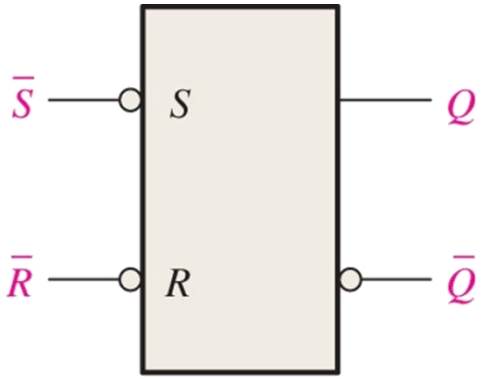


(a) Active-HIGH input S-R latch

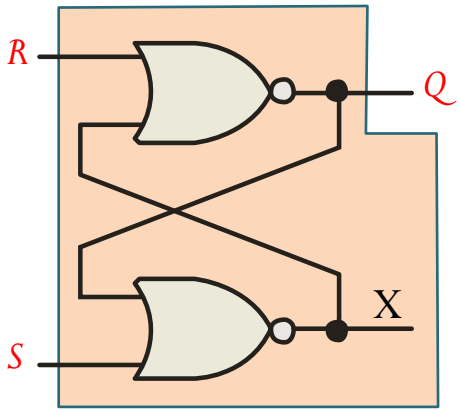


(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch





The “Old Q”-“New Q” Analysis



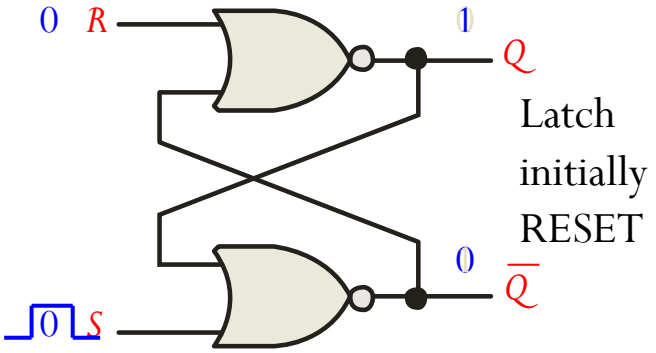
$$Q_{new} = \overline{R + X}$$
$$= \overline{R + \overline{\overline{Q_{old} + S}}}$$
$$= \overline{R} \cdot \left(Q_{old} + S \right)$$

Input		Output
S	R	Q_{new}
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

Active-HIGH S-R latch

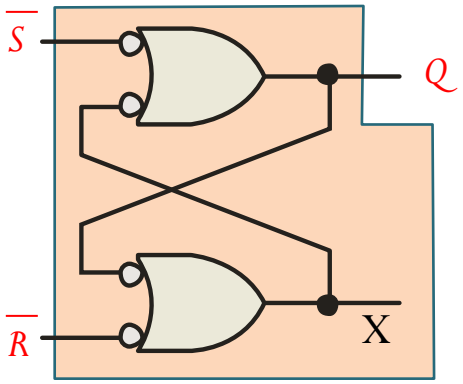
Input		Output
S	R	Q_{new}
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the *S* input while the *R* remains LOW.



To RESET the latch ($Q = 0$), a momentary HIGH signal is applied to the *R* input while the *S* remains LOW.

The “Old Q”-“New Q” Analysis (2)



$$Q_{new} = ?$$

Input		Output
$\overline{S}$	$\overline{R}$	Q_{new}
0	0	
0	1	
1	0	
1	1	